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FOR IMMEDIATE RELEASE

SYMPHONY EDA INTRODUCES HIGH-PERFORMANCE VHDL SIMULATOR; SETS NEW STANDARD FOR REDUCING COSTS OF FPGA AND ASIC DESIGN VERIFICATION

BEAVERTON, Ore., June 21, 2005 -- Symphony EDA today announced the release of VHDL Simili™ 3.0, a complete VHDL simulation software environment that significantly reduces verification cycle time in complex chip designs while lowering the cost of ownership for high-performance simulation tools.

VHDL Simili 3.0 offers extensive simulation performance optimizations, source-level debugging capability, fast code coverage analysis and reporting, full language support including Vital and SDF, an integrated development environment, and platform support for Windows and Linux. The feature set of VHDL Simili 3.0 enables flexible and efficient verification of multi-million gate ASIC and FPGA based designs.

“As FPGA and ASIC design complexity continues to grow, the percentage of engineering cycle time spent in simulation and verification tasks is actually growing,” said Haneef Mohammed, President and CTO of Symphony EDA. “With VHDL Simili 3.0, we have cultivated the key simulator features that are crucial to

improving design productivity – namely performance, user interface, debugging capability, and RTL coverage. We feel that these kinds of critical improvements in productivity should be more accessible to the design community at large."

Both RTL and gate-level customer designs that have been run on VHDL Simili 3.0 have realized between 2X and 8X gain in performance over previous simulator releases. This can be attributed to Symphony EDA's second-generation ZEOS (Zero-Overhead-Stack)™ technology, which enables very fast, on-the-fly language interpretation and simulation kernel execution in VHDL Simili 3.0, as well as high-impact performance optimizations such as Level-0 and Level-1 Vital model acceleration.

VHDL Simili 3.0 provides valuable code coverage analysis for RTL verification, and does so with very low overhead (less than 5% performance penalty). The tool supports advanced debugging features such as breakpoints, flexible line-stepping, and signal force/release. Furthermore, VHDL Simili 3.0 employs an industry-leading user interface as part of its integrated development environment (Sonata™) – including an intuitive and feature-rich waveform viewer, a VHDL-aware design editor, automatic hierarchy detection and file ordering, smart compliation, and a Tcl console for scripting.

Symphony EDA differs from most EDA tool vendors by offering one-year renewable licenses for their products which include free upgrades and technical

support, instead of a perpetual licensing model where the up-front costs may be multiplicatively higher and are followed by sizeable annual maintenance charges to enable tool upgrades and support. “Certainly, design productivity also increases when a customer can increase their number of simulation licenses by 2 or 3 times for the same amount of dollars allocated in their budget, or can spend the cost difference elsewhere to accelerate their design cycle,” says Mohammed.

Pricing and Availability

VHDL Simili 3.0 is available now for download at http://www.symphonyeda.com. A one-year renewable license, inclusive of all tool upgrades and technical support, starts at $750 for VHDL Simili 3.0 Professional Edition. Multiple licensing options are available.

About Symphony EDA

Symphony EDA, based in Beaverton, Oregon, is a leader in HDL simulation technology and has been providing commercial simulation tools to the industry since 2003. Symphony EDA produces verification solutions that are “the tools of choice of the FPGA and ASIC engineer” by focusing on fundamental design productivity needs such as performance, correctness, and interface, and pioneering advanced technologies that meet and exceed those needs. For more information on Symphony EDA products or company profile please email sales@symphonyeda.com or visit http://www.symphonyeda.com.

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